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United States Patent	5,961,791
Frisa , et al.	October 5, 1999

Process for fabricating a semiconductor device

Abstract

A via 42 is formed in an ILD layer 40 of a semiconductor device 30, using an etch chemistry which is highly selective to an underlying transition metal oxy-nitride film 38. In one form, film 38 is a $TiO_x N_y$ film which is graded in nitrogen and oxygen concentration, being nitrogen rich at the bottom and oxygen reach at the top of the film. One method for forming $TiO_x N_y$ is to sputter deposit a titantium layer 34 onto the semiconductor device using a titanium target 52. Using the same target, a TiN layer 36 is deposited by flowing nitrogen into the deposition chamber. Consequently, a TiN layer 58 is deposited onto target 52. The TiN layer 58 is then sputtered off the target onto the semiconductor device until eventually pure titanium is again being sputtered onto the device. The resulting deposited film has a grade titanium concentration, whicb is then oxidized to form the graded $TiO_x N_y$ film.

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Claims

We claim:

1. A process for fabricating a semiconductor device comprising:

providing a conductive substrate;

depositing a first layer on the conductive substrate, the first layer comprising a first material;

depositing a second layer on the first layer from a target, the second layer comprising a second material, wherein:

the second layer is different from the first layer; and

the target is coated with the second material;

depositing a third layer on the second layer from the coated target, the third layer being graded with increased content of the second material toward the second layer and increased content of the first material away from the second layer;

oxidizing the third layer;

depositing a fourth layer on the third layer; and

forming at least one via selectively through the fourth layer to the third layer, wherein the at least one via exposes a portion of the oxidized third layer.

2. The process of claim 1 wherein the first material includes a transition metal material.

3. The process of claim 1 further comprising removing the exposed portion of the oxidized third layer.

4. The process of claim 1 wherein the conductive substrate includes an aluminum material.

5. The process of claim 1 wherein the conductive substrate includes a transition metal material.

6. The process of claim 1 wherein:

the fourth layer is an interlayer dielectric layer; and

while forming the at least one via, an etch chemistry is used, wherein an etch rate ratio of the third layer to the fourth layer is greater than 40:1.

7. The process of claim 1 wherein oxidizing comprises:

activating oxygen in a plasma environment; and

flowing the oxygen downstream to oxidize the third layer.

8. The process of claim 1 wherein oxidizing is performed in a wet chemical environment.

9. The process of claim 1 wherein oxidizing is performed in an ozone environment.

10. The process of claim 1 wherein oxidizing is performed at a temperature below which the conductive substrate melts.

11. The process of claim 10 wherein the temperature is no greater than 450.degree. C.

12. The process of claim 1 wherein removing the exposed portion comprises sputtering in a plasma environment.

13. The process of claim 1 wherein removing the exposed portion is performed in a wet chemical environment.

14. The process of claim 1 wherein the conductive substrate includes copper.

15. The process of claim 14, wherein the first material includes tantalum.

16. A process for fabricating a semiconductor device comprising:

providing a substrate having a metal interconnect;

depositing a first layer on the substrate, the first layer comprising a first material;

oxidizing a top portion of the first layer, the top portion is graded with increased oxygen content away from the substrate, wherein oxidizing is performed at no greater than 450.degree. C.;

depositing a second layer on the top portion of the first layer; and

forming a via selectively through the second layer to the top portion of the first layer, wherein in forming the via, an etch chemistry is used wherein etching stops within the top portion of the first layer.

17. The process of claim 16 wherein the first material includes a transition metal material.

18. The process of claim 16 wherein the metal interconnect includes an aluminum material.

19. The process of claim 16 wherein the second layer is an interlayer dielectric layer of a semiconductor device.

20. The process of claim 16 wherein oxidizing comprises:

activating oxygen in a plasma environment; and

flowing the oxygen downstream to the first layer.

21. The process of claim 16 wherein oxidizing is performed in a wet chemical environment.

22. The process of claim 16 wherein oxidizing is performed in an ozone environment.

23. The process of claim 16 further comprising:

after forming the via removing an exposed part of the top portion of the first layer.

24. The process of claim 23 wherein removing the exposed part comprises sputtering in a plasma environment.

25. The process of claim 23 wherein removing the exposed part is performed in a wet chemical environment.

26. The process of claim 16, wherein the metal interconnect includes copper.

27. The process of claim 26, wherein the first material includes tantalum.

28. A process for fabricating a semiconductor device comprising:

providing a semiconductor substrate having a metallization layer;

depositing a transition metal nitride layer on the metallization layer;

depositing a transition metal layer on the transition metal nitride layer, wherein the transition metal layer is graded with increased content of transition metal nitride toward the transition metal nitride layer and increased content of transition metal material away from the transition metal nitride layer;

oxidizing at least a portion of the transition metal layer to form a transition metal oxide layer;

depositing an interlayer dielectric layer on the transition metal oxide layer;

exposing the transition metal oxide layer by forming a via through the interlayer dielectric layer;

removing an exposed portion of the transition metal oxide layer; and

forming a conductive plug in the via.

29. The process of claim 28 wherein the transition metal oxide layer includes titanium and oxygen.

30. The process of claim 29 wherein transition metal oxide layer further includes nitrogen.

31. The process of claim 28 wherein the metallization layer includes an aluminum material.

32. The process of claim 28 wherein the metallization layer includes copper.

33. The process of claim 28 wherein oxidizing is performed in a wet chemical environment.

34. The process of claim 28 wherein oxidizing is performed in an ozone environment.

35. The process of claim 28 wherein oxidizing comprises performing an oxygen plasma downstream ash operation.

36. The process of claim 28 wherein the oxidizing is performed at a temperature is no greater than 450.degree. C.

37. The process of claim 28 wherein removing the exposed portion comprises sputtering in a plasma environment.

38. The process of claim 28 wherein removing the exposed portion is performed in a wet chemical environment.

39. The process of claim 28 wherein the transition metal is tantalum.

40. The process of claim 28 wherein the transition metal is titanium.

Description

FIELD OF THE INVENTION

The present invention relates generally to methods for making semiconductor devices, and more particularly to methods for forming vias in semiconductor devices.

BACKGROUND OF THE INVENTION

Vias are used in semiconductor manufacturing to connect one level of metallization to an underlying level of metallization. Separating the layers of metal is typically an interlayer dielectric (ILD) which is typically formed of silicon dioxide. In forming a via, an anisotropic etch is performed through the ILD layer to expose an area of the underlying metal. In forming the vias through an ILD layer, the ILD thickness varies considerably across individual wafers and from wafer to wafer and lot to lot. Accordingly, to expose the underlying metallization layer, everywhere, most semiconductor manufacturers perform an overetch of the ILD layer. In other words, the etch of the ILD layer is performed longer than would be required for certain thickness, in an effort to remove the thickest portions of the ILD layer.

FIG. 1 illustrates a portion of a semiconductor device 10 which illustrates the problems associated with over etching the ILD layer. Within device 10 is an underlying metallization layer 12 , which is typically in the form of aluminum or an aluminum alloy. Deposited on top of the aluminum layer is a titanium (Ti) layer 14 and a titanium nitride (TiN) layer 16. Titanium nitride layer 16 serves as an anti-reflective coating (ARC) to aid in the photo lithography process, as is conventionally known. Titanium layer 14 serves as a barrier layer, and lowers the contact resistant in a via which is made to underlying metallization layer 12. Over the metallization stack is formed an ILD layer 18. In a preferred embodiment ILD layer 18 is plasma deposited silicon dioxide. As shown, ILD layer 18 has a planar top surface as a result of chemical mechanical polishing (CMP), as is well known in the prior art. After polishing back ILD layer 18, semiconductor device 10 is patterned and etched to form a via 20 through the ILD layer. In one prior art method, via 20 is formed using a chemistry of CHF.sub.3 and argon either with or without CF.sub.4. With such a chemistry, the ratio of the etch rates between ILD layer 18 and titanium nitride layer 16 is approximately between 10:1 and 15:1. However, such etch rate selectivity is insufficient given that ILD layer 18 can vary in thickness from about 70-80% (i.e. 10,000 angstroms (.ANG.) to 17,000 .ANG.). With such a variation in ILD thickness and such etch rate selectivity, it is impossible to guarantee that the via etch stops somewhere between TiN layer 16 and Ti layer 14. It is very important that the via etch stops between these layers, for exposure of the underlying metallization layer 12, typically in the form of aluminum, is detrimental to subsequent plug formation within via 20. More particularly, conventional practices are to deposit a TiN glue layer within via 20. When aluminum is exposed at the bottom of via 20, nitrogen will react with the aluminum to form aluminum nitride which is undesirable because it will increase the resistance of the contact. Lining via 20 with titanium prior to depositing titanium nitride may prohibit the formation of aluminum nitride. However, any exposed titanium will undesirably react with WF.sub.6, a chemical commonly used to form tungsten plugs within via 20.

One method to assure that the via etch stops before exposing the underlying aluminum metallization is to use an etch chemistry which is highly selective to titanium nitride. A few chemistries have been

proposed, for example helium has been added to the conventional CHF.sub.3 and argon etch process to improve etch selectivity to about 21:1. However, this too is insufficient given the varying thickness of ILD layer 18 across the wafer and from wafer to wafer and lot to lot. Other selective chemistries are C.sub.4 F.sub.8 or C.sub.3 F.sub.8 based chemistries which are more selective to TiN. However, use of these chemistries suffers from the disadvantage that throughput of wafers is relatively low. For example, a typical etch time using these chemistries is 10 minutes per wafer while using a CHF.sub.3 base chemistries is on the order of 4 minutes per wafer. Furthermore, use of C.sub.4 F.sub.8 and C.sub.3 F.sub.8 based chemistries are less reliable processes. In some instances, the etching of ILD layer 18 will stop without having cleared the underlying metallization due to uncontrolled polymer deposition.

Therefore, there is a need for a new process to be able to etch vias within semiconductor devices without exposing the underlying aluminum metallization, while clearing the ILD layer in the vias despite variations in the ILD thickness. Furthermore, it is desirable that such a process is performed without degrading wafer throughput in the factory.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a partial cross-sectional view of a semiconductor device formed in accordance with the prior art.

FIG. 2 is a partial cross-sectional view of a semiconductor device having a via formed in accordance with the present invention.

FIGS. 3-6 illustrate, in sequence, how the metallization stack of the semiconductor device of FIG. 2 is formed in accordance with one embodiment of the present invention.

FIGS. 7-8 illustrate the semiconductor device of FIG. 2 as a plug material and a subsequent metallization layer is formed.

FIG. 9 is a Auger Electron Spectroscopy depth profile of a titanium oxy-nitride film formed in accordance with the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Generally, the present invention provides a method for forming vias in a semiconductor device which utilizes a titanium oxy-nitride (TiO.sub.x N.sub.y) film as an etch-stop layer for a via etch. In accordance with one embodiment of the invention, on top of the traditional titanium and titanium nitride films deposited on aluminum, a graded film containing titanium, oxygen and nitrogen is formed on the surface of the titanium nitride layer. The TiO.sub.x N.sub.y film is graded in oxygen and nitrogen concentration from the bottom to the top of the film, being nitrogen rich near the bottom of the film and oxygen rich near the top of the film. In one embodiment the TiO.sub.x N.sub.y film is formed by sputter depositing a titanium nitride layer which is formed on a titanium target in a sputter deposition tool. After removing the titanium nitride layer of the target, pure titanium is deposited, and this titanium is converted to titanium oxide using a downstream O.sub.2 plasma ash. Oxidizing

titanium in the film serves two purposes: (1) to form a film which can be used as an etch-stop during the via etch process and (2) to serve as an ARC for patterning the underlying metallization layer. By ~~illustrations are not necessarily drawn to scale, and there are likely to be other embodiments of the~~ invention which are not specifically illustrated. For simplicity and clarity reasons, reference numerals are sometimes used throughout the various views to note identical or similar elements.

FIG. 2 illustrates, in a cross-sectional view, a portion of a semiconductor device 30 formed in accordance with one embodiment of the present invention. Device 30 includes an underlying metallization layer 32 which is typically an aluminum or an aluminum alloy, but is not limited to these materials. For example, the underlying metallization may be copper or a copper alloy. Overlying metallization 32 is a titanium layer 34 and a titanium nitride layer 36 as was formed in prior art semiconductor devices. In accordance with the invention, a TiO.sub.x N.sub.y layer 38 is formed on top of titanium nitride layer 36. The method in which TiO.sub.x N.sub.y layer 38 is formed in subsequently described in reference to FIGS. 3-6. After forming TiO.sub.x N.sub.y layer 38, an interlayer dielectric (ILD) layer 40 is formed over semiconductor device 30 in accordance with conventional practices. A via opening 42 is formed within ILD layer 40 using conventional oxide etch chemistries. In accordance with the invention, during the formation of via 42, TiO.sub.x N.sub.y layer 38 serves as a very effective etch-stop, such that during the etch of via 42, the etch will stop on or in TiO.sub.x N.sub.y layer 38, without breaking into the underlying metallization layer 32.

FIGS. 3-6 illustrate a method for forming the titanium, titanium nitride, and TiO.sub.x N.sub.y layer of semiconductor device 30 in accordance with a preferred embodiment of the present invention. Shown in FIG. 3 is a semiconductor device substrate 30 within a sputter deposition chamber 50. Semiconductor device 30 is placed within the chamber, along with a sputter target 52. In practicing the present invention, any type of sputter deposition tool may be suitable for depositing the various layers, with the Applied Materials Endura system being an example of one suitable tool. While only a portion of semiconductor device 30 is shown in FIGS. 3-6 for purposes of clarity, one of ordinary skill in the art will recognize that typically an entire wafer will be placed within the sputter deposition chamber of such tool.

Once a device is within the chamber, an argon plasma, represented in FIG. 3 by plasma 54, is generated. During a sputter deposition process, argon ions from plasma 54 hit target 52 and deposit the target material on to semiconductor device 30. In a first deposition step, a thin titanium layer 34 is

deposited from a titanium target, being about 50 to 300 .ANG. thick.

After depositing titanium layer 34, titanium nitride layer 36 is deposited on device 30 within the same deposition chamber 50, as shown in FIG. 4. To deposit titanium nitride film rather than a pure titanium film from the pure titanium target 52, a nitrogen gas 56 is introduced into the chamber along with the argon gas to form a nitrogen-argon plasma 56. Alternatively, nitrogen alone can be used. Positive ions from plasma 56 impinge upon target 52, but rather than pure titanium being deposited on substrate 30, the titanium atoms react with the nitrogen to form titanium nitride which is deposited onto the device. Deposition of titaninm nitride is continued until the desired thickness is achieved. In a preferred embodiment of the present invention, titanium nitride layer 36 is deposited to a thickness between 400-1000 .ANG..

As FIG. 4 also shows, during the formation of titanium nitride layer 36, a titanium nitride layer 58 forms on target 52. This is the natural consequence of using a pure titanium target to deposit titanium nitride film using nitrogen gas. Not only will titanium nitride deposit on a semiconductor device but it will also form upon the titanium target. In prior art processes, titanium nitride layer 58 must be removed in order to process the next wafer within sputter deposition chamber 50. Since pure titanium is the first layer to be deposited within the chamber , titanium nitride layer 58 must be removed to expose the pure titanium target. Otherwise, deposition of titanium nitride will occur until the layer is completely removed, thereby, exposing the pure titanium target. One method for removing titanium nitride layer in the prior art is to use what is know as a "shutter disk" such as that provided with an Applied Materials Endura sputter deposition system. Alternatively, a sacrificial wafer could be used in place of the shutter disk. After depositing titanium and titanium nitride on one semiconductor substrate, the shutter disk is placed within deposition chamber 50, and titanium nitride layer 58 it sputtered off the target using argon plasma 54, and deposited onto the shutter disk. The shutter disk is then removed and the next semiconductor substrate is placed within the deposition chamber. A pure titanium film can then be deposited upon the next substrate.

In accordance with the present invention, titanium nitride layer 58 which is formed on the target is actually used to form TiO.sub.x N.sub.y layer 38. As shown in FIG. 5, semiconductor device 30 remains within deposition chamber 50 for formation a graded TiN.sub.y film 37, which will ultimately become TiO.sub.x N.sub.y layer 38. After depositing the titanium nitride layer 36, the nitrogen gas flow is turned off, and only an argon plasma 54 remains. Argon ions from the argon plasma sputter away titanium nitride film 58 on target 52 causing deposition of titanium nitride onto semiconductor device 30. As the titanium nitride layer 58 is removed from target 52, the composition of the layer being deposited onto semiconductor device 30 changes, becoming richer in titanium as deposition progresses. In other words, as initially deposited, the layer will be nitrogen rich, with decreasing content of nitrogen through the thickness of the film, and so ultimately pure titanium is being deposited. In reference to FIG. 5, a graded TiN film 37 is deposited as a result of this process wherein the lower portion of the graded film is nitrogen rich, while the upper portion of the film is titanium rich. Because graded TiN.sub.y film 37 is formed on semiconductor device 30 in accordance with the present invention, the need to use the shutter disk or sacrificial wafer as was used in the prior art is eliminated, thereby reducing processing time.

After forming graded TiN.sub.y 37, this layer is oxidized in a next step as illustrated in FIG. 6.

Semiconductor device 30 is placed in an active oxygen environment which will convert a titanium rich portions of the graded TiN.sub.y layer 37 into titanium oxide. In one embodiment of the present invention, this oxidation process is achieved by performing a downstream O.sub.2 plasma ash for 30-90 seconds. The oxidation is a self limiting reaction such that continued ashing will not produce additional titanium oxide. Another method for oxidizing the titanium is to expose the semiconductor device to ozone. A feature with the oxidation process is that it should not occur at temperatures which are incompatible with the underlying metallization. For example, when using aluminum, an oxidation process should be kept below 450.degree. C. As shown in FIG. 6, TiO.sub.x N.sub.y layer 38 is again divided into a lower and upper portion. Because the oxidation is a self-limiting step, and oxygen will not react with TiN, a lower portion of TiO.sub.x N.sub.y layer 38 will be nitrogen rich, while the upper portion of the layer will be oxygen rich. An example of the composition of TiO.sub.x N.sub.y layer 38 is shown in FIG. 9, which is an Auger Electron Spectroscopy (AES) depth profile of layer 38. As is shown in FIG. 9, the top most surface layer 38 is richer in oxygen than in nitrogen, while the bottom of the film (at approximately 150 .ANG.) is richer in nitrogen. It is noted that the graph shown in FIG. 9 represents TiO.sub.x N.sub.y layer which was formed directly on a silicon substrate. Accordingly, at depths greater than 150 .ANG., silicon is the only species being detected by AES.

The purpose of converting the graded TiN.sub.y 37 to a TiO.sub.x N.sub.y layer 38 is three-fold. One reason is that titanium oxy-nitride will serve as a much more effective etch-stop layer than titanium nitride. A second reason is that titanium by itself is too reflective to serve as the upper most layer of the metalization. By converting the upper most titanium layer to TiO.sub.x N.sub.y, the reflectivity is greatly reduced, aiding in subsequent photolithography operations. Thirdly, by converting the titanium to titanium oxy-nitride, the upper most film is chemically stable for subsequent processing steps.

After forming TiO.sub.x N.sub.y layer 38, semi-conductor device 30 can continue in the fabrication process in accordance with conventional practices. As illustrated in FIG. 7, an interlayer dielectric 40 is deposited over the device and via 42 is formed in ILD layer 40 in accordance with conventional practices. For example, a CHF.sub.3 and argon chemistry, either with or without CF.sub.4, can be used to form via 42 in ILD 40. In accordance with the present invention, the via etch stops on or in TiO.sub.x N.sub.y layer 38 due to the selective nature of the etch chemistry to titanium oxy-nitride.

After forming via 42, the plug metalization is ready to be deposited within via 42. According to conventional practice, a via glue preclean is performed using an argon sputtering process. Traditionally, such a preclean is used to clean up the surface of the underlying titanium nitride film which is exposed at the bottom of via 42. In accordance with the present invention, the same argon sputter preclean can be used to remove TiO.sub.x N.sub.y layer 38 from the bottom of via 42. Layer 38 is removed from the bottom of the via for sufficient contact to the underlying metallization. In accordance with the present invention, a removal of about 100 .ANG. of TiO.sub.x N.sub.y layer 38 results in adequate contact resistance. This number is likely to vary depending upon the time one sputters the titanium target in forming the graded TiN.sub.y layer 37. The longer such sputtering occurs, the more titanium will be on the surface of the device that needs to be removed. If the titanium layer is too thick, some titanium remains unoxidized, and it is undesireable to leave unreacted titanium along the sidewall because it is chemically unstable.

After the glue preclean, a glue layer 60 is deposited over semiconductor device 30. Initially, glue layer

60 will be deposited over ILD 40 and into via 42. Next the ~~layer fill~~ ~~~~~~~~

and higher distribution of via resistance. In a preferred embodiment, the etch rate ratio between the ILD layer and the transition metal oxynitride is greater than 45:1. Furthermore, use of the TiO.sub.x N.sub.y layer allows a simple timed via etch process to be used, despite there being a wide variation in ILD thickness. Accordingly, the present invention is quite suitable for use in a processes utilizing chemical mechanical polishing in the interlayer dielectric. Moreover, use of the present invention actually increases throughput in the semiconductor manufacturing process. The most significant throughput enhancement is the fact that use of a shutter disk or sacrificial wafer in depositing titanium and TiN films in the same deposition chamber using a titanium target is completely eliminated. Accordingly, the 30 second to 60 second target cleaning process is eliminated between each wafer. Furthermore, use of the present invention enables a thinner TiN layer to be deposited as an ARC layer over the metallization, thereby reducing the deposition time of such film. A thinner TiN film also results in less film stress, and thereby lessens the probability of aluminum extruding into the via. A thinner TiN layer also reduces the amount of photoresist needed to pattern the underlying metalization layer, thereby saving material costs. Additionally, the present invention is achieved with no additional processing steps, if an O.sub.2 ash is performed prior to depositing photoresist for deep ultra violet (DUV) lithography. Furthermore, the entire process can be performed at temperatures which are compatible with the underlying metalization scheme, for example below 450.degree. C.

Thus it is apparent that there has been provided in accordance with the present invention, a method for forming vias in a semiconductor device that fully meets the needs and advantages set forth previously. Although the invention has been described and illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to the illustrative embodiments. Those skilled in the art will recognize that modifications and variations can be made without departing from the spirit of the invention. For example, the processes previously described can be practiced in conjunction with the use of tantalum films or films of other transition metals. Furthermore, the present invention is not limited to the particular methods for oxidizing the film as those described. For example, wet chemistries can be used to oxidize the film. Furthermore, a wet etch chemistry can be used to remove the oxidized film from within the via opening. Furthermore, any type of sputtering can be used to remove the oxidized film from within the via opening. Therefore, it is intended that this invention encompass all such variations and modifications that fall within the scope of the intended claims.

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| **United States Patent** | **6,524,869** |
| **Satterfield , et al.** | **February 25, 2003** |

Method and apparatus for detecting ion implant induced defects

Abstract

Various methods and apparatus are provided for testing an ion implantation tool. In one aspect, a method of testing an ion implanter is provided that includes forming a mask with a preselected pattern on a substrate. An ion implant is performed on the mask with the ion implanter. Following the ion implant, a scan of the mask is performed to identify any defects thereon. Defects appearing on the mask following the implant are indicative of latent mechanisms at work within the implanter. Ion implanter induced defects may be economically analyzed.

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Claims

What is claimed is:

1. A method of testing an ion implanter, comprising: forming a mask with a preselected pattern on a substrate; performing an ion implant on the mask with the ion implanter; and following the ion implant, performing a first scan of the mask to identify any defects thereon.

2. The method of claim 1, comprising performing a second scan of the mask prior to performing the ion implant to identify any defects thereon existing prior to the ion implant, and comparing the first and second scans to identify any defects appearing on the mask following the ion implant.

3. The method of claim 1, wherein the mask comprises photoresist.

4. The method of claim 1, wherein the mask comprises oxide.

5. The method of claim 1, wherein the mask comprises a plurality of parallel lines.

6. The method of claim 1, wherein the substrate comprises an oxide film positioned on a silicon substrate.

7. The method of claim 1, wherein the first scan is performed with a metrology tool.

8. The method of claim 7, wherein the first scan comprises characterizing any defects found according to defect type.

9. The method of claim 1, wherein the ion implant comprises implanting with a p-type or a n-type impurity species.

10. The method of claim 2, wherein the second scan is performed with a metrology tool.

11. The method of claim 10, wherein the second scan comprises characterizing any defects found according to defect type.

12. The method of claim 2, wherein the comparing of the first and second scans to identify any defects appearing on the mask following the ion implantation comprises defect source analysis.

13. A method of testing an ion implanter, comprising: forming a mask with a pre-selected pattern on a substrate, the preselected pattern mimicking a pattern of circuit structures to be formed in an integrated circuit; performing a first scan of the mask to identify any defects thereon; performing an ion implant on the mask with the ion implanter, the ion implanter being set to implant at conditions corresponding to implant conditions to be used in implanting a region of the integrated circuit including the circuit structures; following the ion implant, performing a second scan of the mask to identify any defects thereon; and comparing the first and second scans to identify any defects appearing on the mask following the ion implant.

14. The method of claim 13, wherein the mask comprises photoresist.

15. The method of claim 13, wherein the mask comprises oxide.

16. The method of claim 13, wherein the mask comprises a plurality of parallel lines.

17. The method of claim 13, wherein the substrate comprises an oxide film positioned on a silicon substrate.

18. The method of claim 13, wherein the first scan is performed with a metrology tool.

19. The method of claim 18, wherein the first scan comprises characterizing any defects found according to defect type.

20. The method of claim 13, wherein the ion implant comprises implanting with a p-type or a n-type impurity species.

21. The method of claim 13, wherein the second scan is performed with a metrology tool.

22. The method of claim 21, wherein the second scan comprises characterizing any defects found according to defect type.

23. The method of claim 13, wherein the comparing of the first and second scans to identify any defects appearing on the mask following the ion implantation comprises defect source analysis.

24. An apparatus, comprising: a substrate; and a mask positioned on the substrate and having a pattern of upwardly projecting members, the members having a base and an upper surface, the base being smaller in cross-section than the upper surface whereby the members are mechanically weaker at their bases than at their upper surfaces.

25. The apparatus of claim 24, wherein the members comprise posts.

26. The apparatus of claim 25, wherein the posts are cylindrical.

27. The apparatus of claim 24, comprising an integrated circuit positioned on the substrate.

28. The apparatus of claim 24, wherein the mask comprises photoresist.

29. The apparatus of claim 24, wherein the mask comprises oxide.

30. An apparatus, comprising: a substrate; and a mask of insulating material positioned on the substrate, the mask having a preselected pattern mimicking a pattern of circuit structures to be formed in an integrated circuit.

31. The apparatus of claim 30, wherein the integrated circuit is positioned on the substrate.

32. The apparatus of claim 30, wherein the integrated circuit is not positioned on the substrate.

33. The apparatus of claim 30, wherein the mask comprises photoresist.

34. The apparatus of claim 30, wherein the mask comprises oxide.

35. The apparatus of claim 30, wherein the mask comprises a laminate of polysilicon and oxide.

36. The apparatus of claim 30, wherein the pre-selected pattern comprises a plurality of parallel lines.

37. The apparatus of claim 30, wherein the substrate comprises an oxide film positioned on a silicon substrate.

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to semiconductor processing, and more particularly to methods and apparatus for testing ion implantation tools for defect mechanisms.

2. Description of the Related Art

The advent of ion implantation marked a major milestone in semiconductor fabrication. Unlike diffusion processes that entail limited control over impurity region geometry and significant consumption of thermal budget, ion implantation promised and delivered the capability of precise geometric positioning of impurity regions with much shallower junctions and without excessive consumption of thermal budget through lengthy anneals. For these reasons, ion implantation has supplanted diffusion in many aspects of impurity region formation in semiconductor processing.

Ion implantation, as the name implies, involves the bombardment of a wafer or substrate surface with a beam of energetic charged atoms or molecules. In currently available ion implanters, the ion beam is formed from a feed source, either a gas or a solid, and accelerated through an acceleration tube. Before striking the target, the ion beam passes through various focusing and scanning apertures. In order to reduce the possibility of charge build up in the implanted surface, a neutralizing beam of electrons is directed into the outgoing ion beam prior to impact with the target surface. The neutralizing beam deionizes a significant quantity of the ions in the ion beam.

Various types of ion implantation processes may be performed at different stages in a given process flow for a semiconductor device. In many cases, the semiconductor wafer undergoes a cleansing bath in which the wafer is subjected to high frequency acoustic pulses. These so-called megasonic baths are designed to liberate contaminants and other unwanted debris left over from the ion implantation and perhaps earlier process steps. A variety of defects have been observed in the circuit structures of semiconductor wafers following megasonic bath cleansing. One type of defect that has been observed some frequency is a missing section or sections of a polysilicon line. Microscopic inspection of such defect sites has revealed that the missing sections are literally torn away from the remaining portions of the polysilicon line. The frequency of such defects has increased as the minimum device geometry or critical dimension of such circuit structures has decreased with improvements in lithography. This at least suggests structural damage due to kinetic collisions as a possible cause for the missing polyline defects.

Latent interactions occurring inside ion implantation tools are suspected as one possible source of the missing polysilicon line defects observed following megasonic bath cleansing. Moving this belief beyond technical suspicion has proved to be difficult. The primary reason is that troubleshooting an ion implantation tool is not a straightforward process. While in operation, ion implantation tools involve a complex interplay of a number of different electric and magnetic fields as well as high velocity spinning parts and particle collisions. The interplay between the various electromagnetic fields, rotating parts and particles within, and the beam geometry, current and energy settings of conventional ion implanters is not well understood.

Conventional methods for investigating the impact of ion implanter settings on wafer defects involve

testing the relationship between tool settings and conditions between defects observed on actual product wafers or on bare silicon wafers. In the former case, actual product wafers are pulled from production and used for the diagnostic. This procedure, of course, requires the scrapping of otherwise useable wafers and therefore involves significant loss of potential revenue. The second technique involving the use of bare silicon as a test structure, while less costly than the aforementioned technique, nevertheless may not exhibit sufficient sensitivity to determine causation of suspected ion implantation induced structural defects. If the suspected ion implantation induced structural defects are dependent upon the topography of the implanted structures, then bare silicon test wafers will not adequately reproduce the conditions faced by actual product wafers.

The present invention is directed to overcoming or reducing the effects of one or more of the foregoing disadvantages.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention, a method of testing an ion implanter is provided that includes forming a mask with a preselected pattern on a substrate and performing a first scan of the mask to identify any defects thereon. An ion implant is performed on the mask with the ion implanter. Following the ion implant, a second scan of the mask is performed to identify any defects thereon. The first and second scans are compared to identify any defects appearing on the mask following the ion implant.

In accordance with another aspect of the present invention, a method of testing an ion implanter is provided that includes forming a mask with a preselected pattern on a substrate such that the preselected pattern mimics a pattern of circuit structures to be formed in an integrated circuit. A first scan of the mask is performed to identify any defects thereon. An ion implant is performed on the mask with the ion implanter with the ion implanter being set to implant at conditions corresponding to implant conditions to be used in implanting a region of the integrated circuit including the circuit structures. Following the ion implant, a second scan of the mask is performed to identify any defects thereon and the first and second scans are compared to identify any defects appearing on the mask following the ion implant.

In accordance with another aspect of the present invention, an apparatus is provided that includes a substrate and a mask positioned on the substrate that has a pattern of upwardly projecting members. The members have a base and an upper surface. The base is smaller in cross-section than the upper surface whereby the members are mechanically weaker at their bases than at their upper surfaces.

In accordance with another aspect of the present invention, an apparatus is provided that includes a substrate and a mask of insulating material positioned on the substrate. The mask has a preselected pattern mimicking a pattern of circuit structures to be formed in an integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

FIG. 1 is a plan view of a semiconductor wafer or substrate in accordance with the present invention;

FIG. 2 is a magnified view of a small portion of FIG. 1 in accordance with the present invention;

FIG. 3 is a plan view of an exemplary embodiment of a test apparatus in accordance with the present invention;

FIG. 4 is a magnified view of a small portion of FIG. 3 in accordance with the present invention;

FIG. 5 is a cross-sectional view of FIG. 4 taken at section 5--5 in accordance with the present invention;

FIG. 6 is a schematic view of an ion implanter and a metrology tool in accordance with the present invention;

FIG. 7 is a plan view of the test apparatus of FIG. 3 following ion implantation and defect scanning in accordance with the present invention;

FIG. 8 is a magnified view of a small portion of FIG. 7 in accordance with the present invention;

FIG. 9 is a cross-sectional view like FIG. 5 of an alternate exemplary embodiment of the test apparatus in accordance the present invention;

FIG. 10 is a plan view like FIG. 4 of another alternate exemplary embodiment of the test apparatus in accordance the present invention;

FIG. 11 is a plan view like FIG. 3 of another alternate exemplary embodiment of the test apparatus in accordance the present invention;

FIG. 12 is a plan view like FIG. 4 of another alternate exemplary embodiment of the test apparatus in accordance the present invention; and

FIG. 13 is a cross-sectional view of FIG. 12 taken at section 13--13 in accordance with the present invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

In the drawings described below, reference numerals are generally repeated where identical elements appear in more than one figure. FIG. 1 depicts a plan view of a semiconductor wafer or substrate 10 upon which a plurality of integrated circuits 12 are fabricated. The wafer 10 is provided with one or more flats 14 or notch(es) (not shown) that facilitate the spatial orientation of the wafer 10 in various semiconductor processing tools. The integrated circuits 12 are delineated into a plurality of die that may be configured to implement any of a variety of electronic functions. Examples include memory circuits, microprocessors, analog-to-digital converters and digital-to-analog converters to name just a

few. The wafer 10 may be composed of silicon, silicon-on-insulator, or other well known substrate materials.

The substrate 10 is shown in FIG. 1 following etch definition of a plurality of circuit structures and defect inspection. The inspection has revealed the presence of various defects, four of which are shown and labeled, respectively, 16, 18, 20 and 22. A small portion of the integrated circuit 12 encompassing the defect 22 is depicted in FIG. 2. As shown in FIG. 2, the integrated circuit 12 includes a plurality of circuit structures. The circuit structures 24 and 26 consist of conductor lines that exhibit a type of structural defect commonly observed following etch definition, ion implantation and megasonic cleaning. The defects consist of damaged or otherwise missing sections 28 of the lines 24 and 26. Similar defects may be observed in insulator structures as well.

The defects 28 have been observed in the circuit structures 24 and 26 of the integrated circuit 12, both before and after megasonic cleaning. However, the number of the defects 28 tends to be markedly higher following megasonic cleaning. Manufacturing experience has demonstrated that the defects 28 tend to appear more frequently, although not exclusively, in relatively long uninterrupted circuit structures, such as the structures 24 and 26. Circuit structures, such as the T-gate structures 30 shown in FIG. 2, have demonstrated fewer occurrences of post-implant and megasonic bath structural failure than those types of circuit structures that do not have intersecting components and/or irregular structural shapes.

The defects 28 are thought to be the result of unanticipated interactions in ion implanters during ion implantation of the integrated circuits 12. In an attempt to track down causation, a novel approach to testing an ion implanter is envisioned. An exemplary method and apparatus in accordance with the present invention may be understood by referring now to FIGS. 3, 4 and 5. A substrate 32 may be provided with one or more die locations 34, and one or more flats 36 or notch(es) (not shown) to facilitate spatial orientation in various processing tools. A mask 38 that has a preselected pattern of structures 40 may be fabricated on one or more of the die locations 34. An exemplary defect 41 on substrate 32 is shown in FIG. 3 and will be described below.

In the embodiment illustrated in FIGS. 4 and 5, the mask 38 consists of a plurality of parallel structures or lines 40 that advantageously mimic the structural topography of, for example, high aspect ratio conductor lines commonly used in commercial integrated circuits. However, the skilled artisan should appreciate that the mask 38 may be patterned in any of a virtually infinite variety of shapes while still achieving the benefits of the present invention. Each of the die locations 34 may be provided with an identical mask 38 or different types of masks may be provided at various die locations 34 as desired.

As best seen in FIG. 5, the substrate 32 may consist of a semiconductor substrate 42 upon which a dielectric film 44, made of, for example, oxide, nitride, or laminates of these is disposed. Although the substrate 32 may be fabricated in any of a great variety of geometries, the substrate 32 may be advantageously fashioned from commercially available wafers that are used for commercial device fabrication.

The substrate 32 is designed to be placed in an ion implantation tool 46 shown in FIG. 6 and subjected

to one or more ion implantation steps. Preferably, the ion implantation steps will be conducted using the same energy, dosage and implant angle implant parameters as used to fabricate circuit structures on a commercial part. In this regard, the implants may be performed using, for example, the same energy, beam current, neutralization current, dosage, impurity specie and implant angle. In this way, the conditions imposed upon the substrate 32 by the implantation tool 46 will closely track those faced by commercial parts.

The mask 38 is advantageously composed of materials that exhibit rigidity and brittleness. These physical properties heighten the probability that the mask structure 38 will exhibit observable structural failure as a result of impacts by massive particles and electrostatic discharge during the ion implantation step. Exemplary materials include, for example, photoresist, polyimide, oxide, polysilicon or the like. Laminate structures are envisioned, such as a stack of polysilicon on oxide. Iu one exemplary embodiment, the mask 38 is composed of I-line photoresist. The mask 38 may be applied to a thickness of about 0.3 to 0.6 .mu.m and the individual structures 40 may be patterned with an aspect ratio of about 2:1 to about 5:1. The skilled artisan will appreciate that the size parameters of the mask 38 are subject to design discretion. If composed of photoresist, well-known resist exposure and bake processes may be employed to fabricate the mask 38.

In order to isolate those surface defects in circuit structures likely caused by latent mechanisms occurring within the ion implanter 46, it may be desirable to determine the pre-implantation state of the substrate 32. Accordingly, the substrate 32 and the mask 38 undergo a pre-implant metrology scan in a metrology tool 48 shown in FIG. 6. The metrology tool 48 may be any of a variety of different types of metrology tools, including commercially available models, such as, for example, a KLA-Tencor AIT laser scanner, a KLA-Tencor 21 XX optical scanner, an Orbot WF laser scanner, or the like, to name just a few. Manual optical scanning may also be used as desired. Indeed, multiple metrology scans in different types of scanners may be used if desired. The metrology tool 48 is provided with a computer system 50 that provides control and data analysis functions. Most commercially available metrology tools include such a computer system for control and data analysis.

An exemplary pre-implant condition for the substrate is depicted in FIG. 3. The results of the scan in the metrology tool 46 indicate the presence of a single exemplary defect 41 on one of the die locations 34. The pre-implant defect(s) 41 may be characterized according to size and type. For example, the defect(s) 41 may be categorized as a surface particle, a missing portion of the mask pattern 38, a surface flake, or other type of defect. These categories represent just a few of the myriad of possible defect categories that may be used.

Following the pre-implant scan, the substrate 32 is placed in the implanter 46 and subjected to one or more ion implantation steps, preferably using the implanter settings energy specified for a particular implant in a commercial product process flow. As noted above, the goal of the implantation step on the substrate 32 is to mimic the conditions that would exist if the substrate 32 were a commercial part undergoing device ion implantation. In an exemplary embodiment, the implantation step is designed to mimic a source/drain impurity implant using arsenic as the impurity specie. The energy may be about 20 KeV and the dosage may be about 4.5E15 ions/cm.sup.2. The implant angle may be 0.degree. and the arsenic may be singly charged. For an implant performed in a Varian Vision 80 implanter, the ion beam current may be about 7 to 9 milliamps and the flood current may be about 3

amps arc current and about 2 sccm xenon gas flow. A slightly higher beam current may be appropriate in, for example, an Applied Materials implantation tool. The implant parameters are subject to design discretion.

A hypothetical post-implant state of the substrate 32 is depicted in FIG. 7. Following the implantation, the substrate 32 and the mask are again scanned in the metrology tool 48. The scan reveals the presence of additional defects 54 located at various die locations 34 on the substrate 32. Note that the post-implant scan of the substrate 32 may be performed before or after a megasonic bath cleaning step. A scan performed prior to megasonic bathing will reveal those defects produced by a structural failure during ion implantation, whereas a scan performed following megasonic bathing will reveal not only those defects associated with a catastrophic structural failure during implant, but also those associated with structural weakening of various circuit structures during ion implant followed by failure during megasonic cleaning.

A magnified view of one of the defect locations 54 is depicted in FIG. 8. The structure 40 of the mask 38 has experienced a structural failure resulting in the missing portion defect 56. The location of the post-implant defect 54 and the other defects may be determined by the computer system 50 using well-known defect source analysis techniques. In this method, the pre-implant defects are subtracted out of a post-implant digital image of the substrate 32. Once located, the post-implant defects 54 may then be analyzed and characterized.

The substrate 32 in accordance with the present invention may, thus, be used to test the implanter 46 as a potential cause for structural defects. The substrate 32 may be implanted at various energy, dosage, implant angle, beam and flood current settings for the implanter and those various combinations of settings may be correlated to defects produced in the masks 38 of the substrate 32. Since the implanter diagnostics may be performed on relatively inexpensive test substrates, circuit defects due to implanter malfunction or contamination may be rooted out at much lower expense.

Two potential causes for ion implanter induced structural defects are thought to be the result of massive particle impacts and electrostatic discharge. Many current ion implanters utilize a relatively large disk that spins at high enough rpms to produce velocities of 200 mph or greater at the outer extremities thereof. It is suspected that such physical extremes may result in the ejection and/or circulation of massive particles that are unintentionally impacted into the surface of semiconductor wafers. Electrostatic discharge is also thought to produce some of the structural defects observed immediately after ion implantation. Both massive particle impacts and electrostatic discharge are thought to at least potentially result from interactions created by automatic tuning and profiling of the ion implantation beam. These automatic tuning and profile adjustment steps are currently carried out just prior to implantation of a given lot of semiconductor wafers. The investigation of the impact of the automatic tuning and profile adjustment for ion beam on the frequency of structural defects in post-implant may be readily investigated using the substrate 32 in accordance with the present invention.

In order to fully investigate the causes of ion implanter induced structural defects in circuit structures, it will be helpful to analyze the composition of massive particles striking a wafer during ion implantation. Experiment has shown that such massive particles tend to exhibit partially inelastic

collisions with circuit structures. Such collisions result in structural failure in circuit structures. However, the collisions tend to be elastic enough so that the suspected massive particles bounce off and remain latent in subsequent metrology scanning. In accordance with another aspect of the present invention, a substrate, now designated 38' and shown in cross-section in FIG. 9, may be fabricated with an overlying mask structure, now designated 38', that consists of a relatively planar sheet. The mask 38' may be composed of the same types of materials used to fabricate the mask 38 depicted above, although softer materials, such as various organic-based glasses, may yield more inelastic collisions and more observable damage than harder materials. In this embodiment, the pre-selected pattern of the mask 38 constitutes a blanket film. The sheet-like construction of the mask 38' provides a large and relatively compliant surface area which can be used to identify impact craters 58 and 60 caused by impacts with massive particles thrown out during the ion implantation process. It is anticipated that a sheet-like mask structure 38' will heighten the chances that a given impact crater, such as the crater 56, will trap a massive particle 60 as shown. The particle 60 may then be excised, cross-sectioned and examined for composition. In this way, a more precise origin of massive particle impacts may be readily determined.

As noted above, the embodiment of the mask 38 shown in FIGS. 4 and 5 represents just one possible configuration. Indeed, the mask 38 may be patterned to mimic the pattern of virtually any circuit structure. FIG. 10 is a plan of an alternate embodiment of the mask, now designated 38", and illustrates just one other possible arrangement.

In the embodiment described above, the mask 38 is implemented on a substrate 32 dedicated to testing. However, the skilled artisan will appreciate that the mask 38 may be incorporated into commercial wafers or substrates. For example, and as shown in FIG. 11, a substrate 62 may be patterned with a plurality of active device die sites 64 and one or more test sites 66. The active device die sites may be provided with one or more integrated circuits. The mask 38 (not visible) may be patterned on the test sites 66 and used to troubleshoot an ion implanter. In this way, only a portion of a commercial wafer need be sacrificed for testing.

In another alternate embodiment depicted in FIGS. 12 and 13, the mask, now designated 38''', is implemented on a substrate 32 with a pre-selected pattern that consists of a plurality of upwardly projecting members or posts 68. FIG. 12 is a plan view and FIG. 13 is a cross-sectional view of FIG. 12 taken at section 13--13. As best seen in FIG. 13, the members 68 are formed with a retrograde, that is, an inwardly sloping profile. This retrograde profile serves two important functions. First, the relatively large upwardly facing surfaces 70 of the members 68 furnish a rich target surface for particle impacts during diagnostic ion implantation. Second, the small cross-sections of the bases 72 of the members 68 translate into diminished mechanical strength. This heightens the chances that a given particle impact will cause a failure in one or more of the members 68 that may be readily observed in post-implant scanning. Other than cylindrical shapes are envisioned for the members 68.

The mask 38''' and the substrate 32 may be fabricated from the same types of materials as the other embodiments described above. If composed of resist, the members 68 may be formed with the retrograde profile by intentionally defocusing the exposure radiation during resist exposure. If composed of other than resist, the retrograde profile may be provided by well-known directional etching techniques in which pressure and chemistry are manipulated during etch to provide a tapering

profile. Implanter diagnostics may be performed with the mask 38''' and substrate 32 using the same techniques described above.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

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Method of detecting crystalline defects using sound waves

Abstract

Various methods of inspecting circuit structures are provided. In one aspect, a method of detecting structural defects in a circuit structure is provided. A natural frequency of the circuit structure is determined and the circuit structure is immersed in a liquid. A first plurality of sonic pulses is sent through the liquid. The first plurality of sonic pulses have a first frequency range selected to produce a plurality of collapsing bubbles proximate the circuit structure. The collapsing bubbles produce a second plurality of sonic pulses that have a second frequency range near or including the natural frequency of the circuit structure whereby the second plurality of sonic pulses causes the circuit structure to resonate. Thereafter, the circuit structure is inspected for structural damage. Early identification of crystalline defects is facilitated.

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Claims

What is claimed is:

1. A method of detecting structural defects in a circuit structure, comprising: determining a natural frequency of the circuit structure; immersing the circuit structure in a liquid; sending a first plurality of sonic pulses through the liquid, the first plurality of sonic pulses having a first frequency range selected to produce a plurality of collapsing bubbles proximate the circuit structure, the collapsing bubbles producing a second plurality of sonic pulses having a second frequency range near or

including the natural frequency of the circuit structure whereby the second plurality of sonic pulses causes the circuit structure to resonate; and inspecting the circuit structure for structural damage.

2. The method of claim 1, wherein the inspecting of the circuit structure comprises electron microscopy.

3. The method of claim 1, wherein the inspecting of the circuit structure comprises optical microscopy.

4. The method of claim 1, wherein the liquid comprises water.

5. The method of claim 1, wherein the liquid comprises a solution of water and ammonium hydroxide or hydrochloric acid.

6. The method of claim 1, wherein the liquid comprises a solution of ammonium hydroxide and hydrogen peroxide in water.

7. The method of claim 1, wherein the determination of the natural frequency of the circuit structure comprises determining a length l of the circuit structure, a speed of sound .nu. through the circuit structure and a density .rho. of the circuit structure, and solving for the natural frequency .nu. according to the below equations where Y is Young's Modulus: ##EQU5##

and ##EQU6##

8. A method of inspection, comprising: determining a natural frequency of a polysilicon line structure; immersing the polysilicon line structure in a liquid; sending a first plurality of sonic pulses through the liquid, the first plurality of sonic pulses having a first frequency range selected to produce a plurality of collapsing bubbles proximate the circuit structure, the collapsing bubbles producing a second plurality of sonic pulses having a second frequency range near or including the natural frequency of the polysilicon line structure whereby the second plurality of sonic pulses causes the polysilicon line structure to resonate; and inspecting the polysilicon line structure for structural damage.

9. The method of claim 8, wherein the inspecting of the polysilicon line structure comprises electron microscopy.

10. The method of claim 8, wherein the inspecting of the polysilicon line structure comprises optical microscopy.

11. The method of claim 8, wherein the liquid comprises water.

12. The method of claim 8, wherein the liquid comprises a solution of water and ammonium hydroxide or hydrochloric acid.

13. The method of claim 8, wherein the liquid comprises a solution of ammonium hydroxide and

hydrogen peroxide in water.

14. The method of claim 8, wherein the determination of the natural frequency of the polysilicon line structure comprises determining a length l of the polysilicon line structure, a speed of sound .nu. through the polysilicon line structure and a density .rho. of the polysilicon line structure, and solving for the natural frequency .nu. according to the below equations where Y is Young's Modulus: ##EQU7##

and ##EQU8###

15. A method of inspection, comprising: determining a natural frequency of a trench structure in a substrate; placing the substrate in a liquid so that at least the trench structure is immersed therein; sending a first plurality of sonic pulses through the liquid, the first plurality of sonic pulses having a first frequency range selected to produce a plurality of collapsing bubbles proximate the trench structure, the collapsing bubbles producing a second plurality of sonic pulses having a second frequency range near or including the natural frequency of the trench structure whereby the second plurality of sonic pulses causes the trench structure to resonate; and inspecting the trench structure for structural damage.

16. The method of claim 15, wherein the inspecting of the trench structure comprises electron microscopy.

17. The method of claim 15, wherein the inspecting of the trench structure comprises optical microscopy.

18. The method of claim 15, wherein the liquid comprises water.

19. The method of claim 15, wherein the liquid comprises a solution of water and ammonium hydroxide or hydrochloric acid.

20. The method of claim 15, wherein the liquid comprises a solution of ammonium hydroxide and hydrogen peroxide in water.

21. The method of claim 15, wherein the determination of the natural frequency of the trench structure comprises determining a length l of the trench structure, a speed of sound .nu. through the trench structure and a density .rho. of the trench structure, and solving for the natural frequency .nu. according to the below equations where Y is Young's Modulus: ##EQU9##

and ##EQU10##

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to semiconductor processing, and more particularly to methods of inspecting circuit structures for structural defects using forced vibration thereof via sonic pulses.

2. Description of the Related Art

Accurate and reliable defect inspection is vital to successful modern integrated circuit fabrication. Many current integrated circuits now routinely contain millions of individual transistors, resistors and other types of circuit components. The patterning of just a few such components on a given circuit may involve scores or even hundreds of different process and wafer movement steps. Therefore, it is desirable to identify defective structural components and fabrication processes so that defective parts may be reworked or scrapped and process recipes adjusted as necessary. Because the processing of an integrated circuit proceeds in a generally linear fashion, that is, various steps are usually performed in a specific order, it is desirable to be able to identify the locations of defects as early in a semiconductor process flow as possible. In this way, defective parts may be identified so that they do not undergo needless additional processing.

The types of structural defects observed in semiconductor circuit structures are legion. One such example is catastrophic structural failure in patterned polysilicon lines. Such patterned structures are used for transistor gate electrodes, local interconnect structures, and power rails to name just a few. The failure mechanisms for such structures vary, and often include an actual rip-out or breaking away of the structure. The origins of such failures may be traced to film contamination, unintended void formation or crystalline defects. Structural weakness in the film due to any of these mechanisms may result in structural failure during processing steps that impart stresses to the wafer, such as thermal shocks associated with bath processes, chemical mechanical polishing, and plasma etching to name just a few.

Conventional techniques for identifying structural defects usually rely on some type of imaging of the structure of interest. Techniques such as optical microscopy, scanning electron microscopy and x-ray diffraction are useful in identifying certain types of structural defects. However, the latter two techniques are generally destructive of the circuit structure and thus require test wafers or sacrifice of the tested wafer, and neither of the three can pick up some types of highly localized or otherwise obscured crystalline defects. These more latent types of defects may not reveal themselves until the integrated circuit is stressed thermally or otherwise much later in a process flow.

The present invention is directed to overcoming or reducing the effects of one or more of the foregoing disadvantages.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention, a method of detecting structural defects in a circuit structure is provided. A natural frequency of the circuit structure is determined and the circuit structure is immersed in a liquid. A first plurality of sonic pulses is sent through the liquid. The first plurality of sonic pulses have a first frequency range selected to produce a plurality of collapsing

bubbles proximate the circuit structure. The collapsing bubbles produce a second plurality of sonic pulses that have a second frequency range near or including the natural frequency of the circuit structure whereby the second plurality of sonic pulses causes the circuit structure to resonate. The circuit structure is inspected for structural damage.

In accordance with another aspect of the present invention, a method of inspection is provided that includes determining a natural frequency of a polysilicon line structure and immersing the polysilicon line structure in a liquid. A first plurality of sonic pulses is sent through the liquid. The first plurality of sonic pulses have a first frequency range selected to produce a plurality of collapsing bubbles proximate the polysilicon line structure. The collapsing bubbles produce a second plurality of sonic pulses that have a second frequency range near or including the natural frequency of the polysilicon line structure whereby the second plurality of sonic pulses causes the polysilicon line structure to resonate. The polysilicon line structure is inspected for structural damage.

In accordance with another aspect of the present invention, a method of inspection is provided that includes determining a natural frequency of a trench structure in a substrate and placing the substrate in a liquid so that at least the trench structure is immersed therein. A first plurality of sonic pulses is sent through the liquid. The first plurality of sonic pulses has a first frequency range selected to produce a plurality of collapsing bubbles proximate the trench structure. The collapsing bubbles produce a second plurality of sonic pulses that have a second frequency range near or including the natural frequency of the trench structure whereby the second plurality of sonic pulses causes the trench structure to resonate. The trench structure is inspected for structural damage.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other advantages of the invention will become apparent upon reading the flowing detailed description and upon reference to the drawings in which:

FIG. 1 is a plan view of a small portion of an integrated circuit patterned on a semiconductor substrate in accordance with the present invention;

FIG. 2 is a cross-sectional view of the substrate of FIG. 1 taken at section 2--2;

FIG. 3 is the cross-sectional view of FIG. 2 depicting one potential mode of structural failure of a portion of the integrated circuit;

FIG. 4 is a cross-sectional view like FIG. 3 depicting another potential mode of structural of portion of the integrated circuit;

FIG. 5 is a side view of a liquid bath suitable for producing vibrations in the integrated circuit of FIG. 1 by sonic pulse propagation in accordance with the present invention; and

FIG. 6 is a side view like FIG. 5 depicting the production of vibrations in a trench structure by sonic pulse propagation in accordance with the present invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

In the drawings described below, reference numerals are generally repeated where identical elements appear in more than one figure. FIG. 1 is a plan view of a small portion of an integrated circuit 10 patterned on a semiconductor substrate 12 in accordance with the present invention. A plurality of conductor lines 14, 16, 18, 20, 22 and 24 are shown and may be patterned as transistor gate electrodes, interconnect lines, or other types of conducting structures frequently used in semiconductor fabrication. Depending upon the requirements of the integrated circuit 10, the conductor lines 14, 16, 18, 20, 22 and 24 may be patterned with a variety of lengths. For example, the conductor line 14 may be fabricated with a length L. The width D of the conductor line 14 may be the minimum feature size for the available process technology or some dimension larger than that as desired. The detailed structure of the conductor line 14 may be understood by referring now also to FIG. 2, which is a cross-sectional view of FIG. 1 taken at section 2--2. An insulating film 26 is formed directly on the substrate 12 and is thus interposed between the conductor line 14 and the substrate 12. This insulating film 26 is customarily a gate dielectric film or a pad oxide layer. The conductor line 14 may be composed of virtually any of a large variety of materials commonly used for integrated circuit conductor structures, such as, for example, polysilicon, amorphous silicon, aluminum, copper, titanium, titanium nitride, tungsten or the like. For the purpose of the present illustration, the conductor structure 14 is composed of polysilicon.

As the skilled artisan will appreciate, crystalline structures, such as the conductor structure 14, may be fabricated with or later develop crystalline defects that substantially reduce the structural integrity of the structure 14. The origins of such defects are legion, and include weak grain boundaries, crystal lattice damage due to impurity implants, impurity contamination, or thermal stresses. The effect is not limited to the conductor structure 14. Indeed, the same types of structural defects may appear in the substrate 12 as well. An exemplary crystalline defect 28 is shown in the conductor structure 14 and another exemplary crystalline defect 30 is shown positioned in the substrate 12 below the conductor structure 14. The defects 28 and 30 represent areas that are prone to structural failure during subsequent processing of the substrate 12. The substrate 12 undergoes a multitude of different processing steps toward the completion of the integrated circuit 10. These processes include, for example, chemical mechanical polishing, various etches, high temperature anneals, and sonic cleaning steps.

Two exemplary failure mechanisms for the conductor structure 14 are depicted in FIGS. 3 and 4, which are cross-sectional views like FIG. 2. Turning first to FIG. 3, the conductor structure 14 has fractured along the defect 28 and essentially ripped away from the remaining portion of the conductor structure 14. Another type of structural failure is depicted in FIG. 4 wherein the entire conductor structure 14 rips away along with a portion of the substrate 12 due to structural failure along the defect 30.

It is desirable to be able to identify the locations of the defects 28 and 30 as early in a semiconductor process flow as possible. In this way, defective parts may be identified so that they do not undergo needless processing that may ultimately result in the types of catastrophic structural failures depicted in FIGS. 3 and 4. An exemplary method in accordance with the present invention for locating defects, such as the defects 28 and 30, may be understood by referring now to FIGS. 1 and 5. As shown in

FIG. 5, the substrate 12 may be immersed in a bath 32 containing a volume of a liquid 34 and subjected to a plurality of sonic pulses 36 from an acoustic source 38. The propagating wave fronts of the sonic pulses 36 strike the substrate 12 and the conductor structure 14 and reflect off. This sets up an interference pattern consisting of positive and destructive interference nodes. At those locations where destructive interference occurs, highly localized areas of low pressure, i.e., cavitation will occur, resulting in the formation of huge numbers of bubbles 40 in the liquid 34. When some of the bubbles 40 impact the surfaces of the conductor structure 14, they collapse, releasing small amounts of kinetic energy in the form of high frequency vibrations. By tuning the parameters of the sonic pulses 36 to the geometry and composition of the conductor structure 14, the bubbles 40 may be generated with a selected collapse period that initiates resonance in the conductor structure 14. The resonance condition will cause structural failure either at the defect 28 or the defect 30 or both. In this way, those structures having defects, such as the defects 28 and 30, may be readily identified so that the substrate 12 does not undergo unnecessary additional processing. The vibration characteristics of the conductor structure 14 may be modeled mathematically in the first instance as a vibrating spring with a spring mass damper. If the structure 14 is subjected to a time-varying input force P sin .omega.t, which corresponds to the input pulses from the collapsing bubbles 40, the equation of motion for the structure 14 is given by:

where x is the displacement of an arbitrarily selected point on the conductor structure 14 from an equilibrium position. In Equation 1, k is the spring constant of the conductor structure 14, m is the mass of the conductor structure 14, c is the actual damping value and .omega. is the frequency of the input force, that is, the frequency of the pulses generated by the collapsing bubbles 40. Note that the expression P sin .omega.t for the time-varying input force of the collapsing bubbles 40 represents an approximation of the actual input force. A Fourier series will provide a more exact representation of the time-varying input force resulting from the combined action of hundreds of thousands or even millions of the collapsing bubbles 40. However, Equation 1 provides a useful approximation to illustrate the present invention.

By performing a Laplace transform on Equation 1, a subsequent algebraic solution thereof, and a follow up inverse Laplace transform, a solution of Equation 1 becomes: ##EQU1##

The damped natural frequency .omega..sub.n of the structure 14 is given by: ##EQU2##

Equation 3 suggests that so long as the damping value c is greater than zero, the conductor 14 will not experience resonance. However, experiments on conductors 14 with lengths of 2.0 .mu.m have suggested resonance induced structural failure. This suggests an under damped condition, that is, that the actual damping value c is quite small, so that Equation 2 yields large enough amplitude x(t) swings to produce failure.

One way to determine the natural frequency .omega..sub.n of the structure 14, and thus the desired input frequency to induce vigorous vibrations in the structure 14, is to assume that the structure 14 mimics the behavior of a stretched string. In such circumstances, the frequency of vibration in the structure 14 is given by the following equation: ##EQU3##

where .nu. is the frequency of vibration, l is the length of the conductor structure 14, .nu. is the

velocity of sound through the conductor structure 14 and n is the harmonic number, e.g., n=1 corresponds to the fundamental harmonic. The velocity of sound in the structure 14 may be determined using the following equation: ##EQU4##

where Y is Young's modulus and .rho. is the density of the conductor structure 14. The velocity of sound through and the density .rho. of the conductor structure 14 will generally be well-known parameters, but may be determined experimentally if necessary.

Experiments were performed on polysilicon conductor structures 14 with conductor lengths l varying from less than 1.0 .mu.m up to several .mu.m. Structural failure was observed in conductor structures 14 with lengths l of 2.0 .mu.m and longer. However, no failures were observed at lengths less than 2.0 .mu.m. This suggests that the 2.0 .mu.m length corresponds to a fundamental harmonic, e.g., n=1, resonant wavelength. Thus, substituting the values of Y, .rho. and l for the conductor structure 14 into Equation 5, yields a resonant frequency .nu. of about 2.0 GHz. Thus, if the input frequency .omega. corresponding to the collapsing of the bubbles 40 is about 2.0 GHz, a resonance condition will be initiated in the structure 14. A resonant frequency of 2 GHz corresponds to a pulse period of about 500 picoseconds.

The collapse time for the bubbles 40 will depend upon a number of parameters associated with the liquid 34, and the sonic pulses 36. The experiments on the 2.0 .mu.m conductors 14 demonstrated that sonic pulses 36 generated with a frequency range of about 950 kHz to 1.5 MHz, and power of about 10 to 300 Watts in the liquid 34 consisting of ultra pure water at a temperature of about 25.degree. C. will produce bubbles 40 with collapse times in a range of 100 to 500 picoseconds. This collapse time range corresponds to a frequency range of about 10.0 to 2.0 GHz, which is suitable to initiate resonance or near resonance vibrations in the conductor 14. While it is desirable for the frequency range of the sonic pulses generated by the collapsing bubbles 40 to encompass the natural frequency .omega..sub.n of the conductor structural 14, it is also anticipated that the conductor structure 14 will undergo rigorous forced vibration where the frequency range is at or near the natural frequency .omega..sub.n.

The sonic pulsing of the conductor structure 14 may be combined with a cleansing bath to remove contaminants or other residues. Indeed, similar diagnostic results may be obtained where the liquid 34 consists of less than 50% solutions of acid or basic solutions, such as HCl or NH.sub.4 OH. Such acid or base solutions may contain up to about 50% by volume H.sub.2 O.sub.2.

As noted above, structural failure was observed in lines having a minimum length of 2.0 .mu.m. Interestingly, structure failures were observed in other lines that had lengths that were integer multiples of 2.0 .mu.m, that is 4.0 and 6.0 .mu.m. This is thought to indicate that the polysilicon lines 14, 16, 18, 20, 22 and 24 (See FIG. 1) are undergoing resonance and second and third harmonics in response to bubble collapse times of about 100 to 500 picoseconds.

Following the sonic treatment of the integrated circuit 10, one or more inspections for structural failures may be performed. The inspection may be by optical microscopy, scanning electron microscopy, infrared scanning, laser scanning or other well-known morphology determination techniques. Indeed any of the above techniques may be performed in concert if desired.

material 46 has an internal defect 48 of the type described above. As with the foregoing illustrative embodiment, the substrate 12 may be immersed in the bath 32 and subjected to a plurality of sonic pulses 36 from the acoustic source 38 that propagate through the liquid 34. The same general procedure outlined above may be used to tailor the parameters of the input sonic pulses 36 in order to achieve a desirable input impulse frequency of the collapsing bubbles 40 to initiate a resonance condition in the trench structure 42. Visual inspection may follow the sonic bath.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

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United States Patent	6,943,569
Pressley , et al.	September 13, 2005

Method, system and apparatus to detect defects in semiconductor devices

Abstract

A method and system to locate and detect voids in films that are involved in critical dimension (CD) structures and non-critical dimension structures in semiconductor devices are presented. One or more test structures (resolution devices) are formed on a semiconductor wafer. A scanning electron microscope is operated in voltage contrast mode to obtain a digital representation of the test structure. The voltage contrast image of the test structure is then analyzed with a system which automates the location, identification, and categorization of voids in the test structure. Additionally, the method is more sensitive to electrical marginalities caused by voids than other wafer electrical testing methods. The method is suitable inline monitoring during a manufacturing process by utilizing the automation of void identification, location, and categorization as a process monitoring parameter.

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Claims

What is claimed is:

1. A method comprising: receiving a digital representation of a structure based on a voltage contrast analysis; transforming the digital representation of the structure along a first axis to create a first one dimensional array; determining a location of a specific portion of the structure based upon the first one dimensional array; transforming a portion of the digital representation along a second axis corresponding to the location of the specific portion to create a second one dimensional array, wherein the first axis is orthogonal to the second axis; and identifying a location of a void based upon the second one dimensional array.

2. The method of claim 1, wherein receiving a digital representation further comprises: receiving a voltage contrast image of the structure; and normalizing a grayscale of the digital representation.

3. The method of claim 1, wherein identifying further includes identifying full void locations.

4. The method of claim 1, wherein identifying further includes identifying partial void locations.

5. The method of claim 1 further comprising: adjusting a manufacturing process parameter based at least partially upon identifying.

6. A system comprising: means for receiving a digital representation of a structure based on a voltage contrast analysis; means for transforming the digital representation of the structure along a first axis to create a first one dimensional array; means for determining a location of a specific portion of the structure based upon the first one dimensional array; means for transforming a portion of the digital representation along a second axis corresponding to the location of the specific portion to create a second one dimensional array, wherein the first axis is orthogonal to the second axis; and means for identifying a location of a void based upon the second one dimensional array.

7. The system of claim 6, wherein the means for receiving a digital representation further comprises: means for receiving a voltage contrast image of the structure; and means for normalizing a grayscale of the digital representation.

8. The system of claim 6, wherein the means for identifying further includes means for identifying full void locations.

9. The system of claim 6, wherein the means for identifying further includes means for identifying partial void locations.

10. The system of claim 6 further comprising: means for adjusting a manufacturing process parameter based at least partially upon the means for identifying.

Description

FIELD OF THE DISCLOSURE

The present invention relates generally to monitoring of of a semiconductor process, and more particularly to the use of an electron beam device in the semiconductor manufacturing industry.

BACKGROUND

The very large scale integration (VLSI) era and, in particular, the 1990s ultra large scale integration (ULSI) circuit integration era require the integration of a million or more circuit components per device (i.e., die). Realizing the ULSI era has required decreasing critical dimensions (CDs) accordingly, and has presented challenges in manufacturing, yield enhancement, and defect detection process areas. As semiconductor geometries shrink, the need for monitoring of critical dimensions (CDs) to achieve precise control over feature size dimensions has grown. The use of optical techniques for monitoring CDs has become less practical, even in the ultraviolet (UV) range, because of the resolution limits inherent with optical diffraction. To overcome the limitations of optical techniques, scanning electron microscope-based inspection processes are generally used for current era integrated circuit critical dimension metrology and defect inspection in wafer fabrication facilities.

In addition to their conventional use to monitor CDs, scanning electron microscopes (SEMs) and electron beam probers, an adaptation of the SEM for functional probing of structures in IC devices, are utilized to obtain voltage contrast images of devices. In a voltage contrast image, the voltage of a structure undergoing imaging determines the brightness of that structure in the image. This is achieved by selective energy filtering to control the detection of secondary electrons, which enhances the voltage contrast. For semiconductor wafers, the SEM voltage contrast method has been proposed for detection of electrical defects that electrically isolate or ground structures.

Various commercial electron-beam wafer inspection systems such as KLA-Tencor's SEMSpec and Analytical Solutions' ISI WB-6 SEM have also been developed to use voltage contrast methods to find "killer" electrical defects and nuisance defects. Killer electrical defects adversely affect the operation of a completed integrated circuit (IC), while "nuisance" defects may not adversely affect the performance of a completed IC. Because nuisance defects are much more numerous than killer defects, it is especially time-consuming to electrically test all of these defects to determine the final performance impact on the IC. KLA-Tencor, Analytical Solutions, and other similar commercial systems have been used in conjunction with digital image processing computers to automate location of killer and nuisance electrical defects, as well as to conduct failure analysis of integrated circuits due to killer and nuisance electrical defects.

However, none of the commercial systems presently available which use the SEM voltage contrast method are configured to purposely detects voids in films, unless the void is of such large dimension that an obvious open or short electrical defect is manifested. However, many voids can be less than 30 nm in size, and are on the order of film roughness dimensions. Small voids in films may result in marginal resistance or resistance gradients between device structures, and give rise to reduced device

performance and reduction in process yields.

Therefore what is needed is a system suitable for inspecting semiconductor wafers in a production environment which provides improved feedback that does not suffer from the known limitations, and which is capable of revealing small hidden voids.

BRIEF DESCRIPTION OF THE DRAWINGS

Other advantages, features and characteristics of the present invention, as well as methods, operation and functions of related elements of structure, and the combinations of parts and economies of manufacture, will become apparent upon consideration of the following description and claims with reference to the accompanying drawings, all of which form a part of the specification, wherein like reference numerals designate corresponding parts in the various figures, and wherein:

FIG. 1 is a simplified block diagram of a system capable of voltage contrast mode operation in accordance with an embodiment of the present invention;

FIG. 2 is a flow diagram of an inline method for detecting voids resulting from various processing methodologies according to at least one embodiment of the present invention;

FIG. 3 is a flow diagram of a method for automation of void identification process according to at least one embodiment of the present invention; and

FIG. 4 is a line drawing symbolizing a serpentine-shaped structure illustrated in plan (top) and cross-sectional views according to at least one embodiment of the present invention.

DETAILED DESCRIPTION OF THE FIGURES

FIGS. 1-4 illustrate a method and system for use in a production environment to locate and detect voids in films that are involved in critical dimension (CD) and non-critical dimension structures, e.g., line widths, thicknesses and spaces, which can cause yield or processor speed degradation in semiconductor devices. In one embodiment, the invention is implemented by the addition of one or more test structures (resolution devices) formed on a semiconductor wafer. A scanning electron microscope (SEM) is operated in voltage contrast mode to obtain a digital representation (i.e., image) of the test structure, and the image of the test structure is then analyzed to locate, identify, and categorize voids in the test structure. While manual identification/categorization of voids in the image of the test structure is possible with reasonable accuracy, a further embodiment of the present disclosure provides a system which automates the identification and categorization of voids on the digital representation of the test structure with a very high degree of accuracy. In the following description, numerous specific details are set forth to provide a thorough description of the invention. However, it will be apparent to one skilled in the art that the invention may be practiced without these specific details, or with other specific details. In other instances, well-known features have not been described in detail so as not to obscure the invention.

Referring to FIG. 1, a simplified block diagram of a system capable of void detection using voltage

contrast mode operation is depicted, and designated generally by reference numeral 100. The illustrated embodiment of system 100 includes an electron microscope sub-system 110, which further includes an electron beam source 120, a focusing column and lens assembly 130, a scan controller 140, a specimen stage 170, an electron detector 160, and an image storing, processing and display sub-system 150. Void ID and categorization portion 180 is illustrated as a stand-alone application receiving a signal 179 from image storing, processing and display system 150 in FIG. 1, however, void ID and categorization portion 180 could be incorporated into image storing, processing and display sub-system 150 as an additional capability of image storing, processing and display sub-system 150 if desired. Void ID and categorization portion 180 may also employ separate processing, display and storage systems, which are not illustrated in FIG. 1. For example, void ID and categorization portion 180 could include a computer workstation for processing data received from image storing, processing and display sub-system 150, with subsequent data analysis output from void ID and categorization portion 180 to a manufacturing database or an historical database, or to a monitor or printer.

During operation, electron beam source 120 is used to generate an electron beam 145, which is focused by focusing column and lens assembly 130. Scan controller 140 is used to scan electron beam 145 across selected regions of specimen 175. The specimen stage 170 supports a specimen 175. Specimen 175 may be comprised of a variety of materials, with the present disclosure particularly applicable to semiconductor materials, e.g., wafers. Small area 176 of specimen 175 is illustrated to indicate that a particular area of interest, e.g., a die, or a portion of a die, or a test structure, can be examined to ascertain features of the specimen 175 in the image of small area 176. Electron detector 160 detects the secondary and/or backscatter electron signal 177 from specimen 175 or small area 176. Electron detector 160 may be of various types that are well known in the art, e.g., semiconductor diode, scintillator/photomultiplier assembly, micro-sphere plate, etc. When electron signal 177 is received by electron detector 160, signal 277 is sent to image storing, processing, and display sub-system 150 for processing, data storage and/or display.

In various embodiments of the present disclosure, small area 176 is a structure such as a poly silicon test structure having a serpentine shape, or N+ or P+ doped poly silicon structures. In a preferred embodiment, digital representations (images) of these various structures obtained from image storing, processing and display sub-system 150 are analyzed by void ID and categorization system 180 to automatically detect and categorize ultra small film voids at or below a critical dimension (CD), which may range from about 1 to about 50 nm. These ultra small film voids are undetectable with conventional detection means. As line widths in devices are reduced below 80 nm, these ultra small voids in, for example, metal silicide and salicide films, will limit the operating speed of the devices, as well as adversely impact device yield during manufacture. Embodiments of the method are eminently suitable for conducting quantitative, inline evaluation of front end of line (FEOL) processes, i.e., operations performed on a wafer during the course of manufacturing up to first metallization, as well as back end of line (BEOL) processes (those processes occurring after first metallization). For example, the method can be employed to detect voids that cause resistance marginalities or gradients in semiconductor device films due to void generation during processing methodologies such as silicide formation, salicide conversion, rapid thermal anneal (RTA) processing, copper films, seed barrier films, electroplated films, chemical vapor deposition (CVD) films, plasma vapor deposition (PVD) films, diffusion films, gate oxide films, etched films, wet-cleaned films, and others well known

in the art. The method can detect very small voids in conducting films, insulating films, isolation oxides, interlayer dielectric films, semiconducting films, e.g. Si, GaAs, superconducting material films, e.g., YBCO films such as YBa.sub.2 Cu.sub.3 O.sub.7, and bulk material films, e.g., Cu, Al . In a variety of cases, e.g., insulating films and salicide films, the method provides an easier, more efficient means of detecting voids and their corresponding electrical marginalities than other methods currently employed in the industry.

Referring to FIG. 2, a flow diagram of an inline method for detecting voids resulting from various processing methodologies, is presented. It should be noted that although the steps in FIG. 2 are described in a sequential order for purposes of illustration, some steps may be performed simultaneously with other steps, or some steps may be performed in a different order than shown in FIG. 2. It should also be noted that although the example presented with FIG. 2 references a test structure in the discussion of the method, functional components of the actual device, i.e., wires or lines comprising a specific portion of the die, could also be used to practice the method. It should be noted, however, that a sheet of film, a portion or portions of a film sheet, or an entire film sheet prior to patterning operations can serve as the test structure to detect voids according to the teachings of the present disclosure. Therefore the use of the phrase "test structure" and the examples presented herein are not meant to limit the application of this method to a specific shape or fabrication process occurrence during manufacture.

The method comprises forming a film over a semiconductor substrate in step 200. This film will serve as the test structure after patterning and etching in step 210. The film may include any material whose properties would serve as an indicator of manufacturing circumstances or processing methodologies. For example, in an embodiment where semiconductor devices undergoing manufacture utilize a dual damascene copper process, the film material of choice for the test structure would be a film containing a copper alloy. As a further example, in embodiments wherein semiconductor devices employ cobalt silicide, nickel silicide, and the like during manufacture, the film material of choice could be material such as poly silicon, N+ doped poly silicon, or P+ polysilicon for the test structure.

In step 210, the film is patterned and etched to form a structure that will serve as a test structure for inline monitoring of process methodologies. Experiments conducted with various test structure shapes during semiconductor device manufacturing has shown that a test structure with serpentine features works very well, primarily due to its large surface area. It should be noted, however, that test structure shapes other than serpentine may be utilized to practice the teachings disclosed herein. For example, some factors to consider when deciding upon a structural form or shape to use as a resolution device (test structure) are the size, i.e., critical dimension, and the characteristics of the material(s) used to fashion the resolution device structure. Generally, the critical dimensions of the features of the structure should be in the range of from about 1 to about 50 nm. Various patterning and etching techniques known to those of skill in the art can be used to produce the appropriate critical dimensions of the features of the structure. Test structures may be placed on any available free space at die sites on a semiconductor wafer. The total number of test structures to place at different die sites on a wafer can range from only a few to one test structure per die site, depending upon how many sampling sites are needed or desired. For mature processes, fewer test structures are generally needed, while processes that are not mature may require the use of many test structures for process monitoring.

In step 215, a wafer with test structures located thereon is placed in the SEM system for inspection in the voltage contrast mode. Voltage contrast data, which forms a digital representation (image) of the test structure, is acquired and/or stored by the imaging sub-system of the scanning electron microscope in step 220. While the analysis herein is described with reference to a specific test structure, the voltage contrast SEM technique disclosed herein can also be be used to analyze a sheet of film or a portion of a film sheet wherein the film sheet is of a material or materials which will ultimately have the desired features, i.e., critical dimension features. In step 225, the digital representation (image) of the test structure is reviewed to detect voids in the film of the test structure. The image of the test structure may be obtained from the imaging sub-system of the SEM, or from the embodied void ID and categorization portion of the SEM system. Voids in the film of a test structure may be manually quantified, as in step 235, or by the automated process of void ID and categorization system, as in step 230. Whether done manually or by automation, void quantification not only counts the total number of voids in the film of the test structure, but also categorizes the voids as one of two types: full voids, and partial voids. Full voids transverse completely across a feature in the test structure, while partial voids partially extend across a feature in the test structure. Full voids produce high resistance and are deleterious to yield, while partial voids may have a lesser effect on yield.

Manual quantification of voids in test structures as in step 235 is typically accomplished by contamination free manufacturing (CFM) personnel examining SEM photomicrographs of features in a test structure obtained in step 220. The CFM methodology attempts to quantify the integrated effects of full and partial voids by employing the concept of a "kill" rate, which is calculated as follows:

Average No. Voids/Die=[(No. Full Voids)+((No. Partial Voids)(X)]/Total Die Inspected

Where X is a yield weighting factor of non-interger value, i.e.,0.26. Typically X is derived from another, similar (known) defect's value from the known defect's yield weighting factor.

While the manual quantification of voids in step 235 is possible with a reasonable degree of accuracy, the process can be time consuming and subject to interpretation errors by the person characterizing the data. A preferred embodiment is to utilize an automated process such as the embodied void ID and categorization portion of the SEM system to quantify the number of voids in the test structure, as in step 230, due to time savings and greatly increased accuracy over manual methodology.

Void ID and categorization analysis of voltage contrast data of test structures as disclosed herein may be conducted at various time splits during a manufacturing process to determine which part or parts of a manufacturing process results in unacceptable yields. Thus, the embodied method can serve as a highly accurate technique for efficient inline process monitoring and process development, as well as yield enhancement. Should the analysis of step 230 or step 235 reveal that some aspect of a manufacturing process results in an unacceptable level of voids in a test structure, or reveals changes that have occurred in an unacceptable manner (and hence voiding or changes to the device which the test structure serves to monitor), in step 240 manufacturing process parameters may be adjusted as necessary. After manufacturing process adjustments in step 240, the procedures of steps 200 through 230 could be repeated until an acceptable outcome is reached.

A further benefit of the disclosure embodied herein is that the method may be used to correlate voids

detected in the film of a test structure with marginalities or resistivity gradients in semiconductor devices detected when a wafer undergoes a wafer electrical test (WET), as in step 245. Experiments with wafers containing the test structures as disclosed herein have revealed a definitive correlation between inline detected film voids and electrical marginality data obtained from wafer electrical testing. Wafer electrical test measures the electrical parameters (i.e., resistance, leakage current, continuity, etc.) of integrated circuits at the wafer level, generally to verify conformity to operational specifications. Wafers typically undergo electrical testing after FEOL processing (after first metal layer deposition and etch), as well as after BEOL processing (completion of manufacturing). Inline parametric tests generally use standard test structures for conducting these parametric tests. These WET test structures are commonly placed in the scribe line regions of a wafer, and are also used for process monitoring and control.

After performing steps 200 through 230 with a test structure as disclosed herein, electrical test measurements were conducted using the embodied test structure. Results indicated a strong correlation exists between yield limiting or speed limiting voids detected according to the present invention and electrical resistivity data obtained from electrical tests on the embodied test structure. A strong correlation also was found between total voids (full and partial voids) and electrical resistivity data with the embodied test structure. Correlation also exists between partial voids detected and electrical resistivity data with the embodied test structure. Hence the method as disclosed herein may be used to adjust a manufacturing process based upon the correlation data, as shown in step 250. Although film voids in a test structure may vary considerably in dimension, they are still detectable using the techniques disclosed herein. Experiments on salicides and doped polysilicon have demonstrated that the embodied method has greater sensitivity to electrical marginalities caused by voids than other wafer electrical testing methods. In a non-conductive film, conventional WET methods usually cannot detect partial voids, only full voids which result in shorting or large resistance changes. Because the present invention reveals a strong correlation between total voids and resistivity, it is a more sensitive metric for device performance and yield than is electrical wafer test data obtained by conventional methods, particularly in the case of salicides or other non-conductive or insulating films. In addition to increased sensitivity over current wafer electrical testing methods, the present invention also provides faster feedback to the process engineer than is possible through conventional electrical testing methods.

Details of the data automation process of the embodied method are presented with reference to FIG. 3 and FIG. 4. FIG. 3 is a flow diagram of a method for automation of void identification according to an embodiment of the present disclosure. FIG. 4 is a line drawing symbolizing a photomicrograph of a serpentine-shaped structure 400 according to an embodiment of the present invention. As previously discussed, use of a serpentine shape is not necessary to practice the teachings of the present disclosure, however, for purposes of example to illustrate the technique, a serpentine-shaped structure 400 with extended run line features 405 and short run line features 410 (as viewed from left to right) representing poly silicon wires on a substrate is shown in FIG. 4. Lines 412 are a portion of extended run line features 405. Again, recall that the choice of material for the structure should be representative of the manufacturing process to be monitored, and therefore the use of poly silicon wire as line features 405, 412, and 410 in FIG. 4 is merely to serve as an example.

Referring to FIG. 3, in step 300, a digital representation (photomicrograph image data) of the structure

to be analyzed, such as structure 400, is received and loaded into an array by the void ID and categorization portoin of SEM system (FIG. 1, item 180). The digital representation may be retrieved from an historical database, an engineering database, or any other database to which the tool (i.e., SEM) sends voltage contrast data (photomicrograph images). As used herein, the term array refers to computing. In computing, an array has its own name or identifier, and each member of the array is identified by a subscript used with the identifier. An array can be examined by a computer program and a particular item of information extracted by using this identifier and subscript.

After loading in step 300, the grayscale of the photomicrograph image (digital representation) is normalized in step 310 by executing a series of instructions to set the minimum pixel value to zero, then to set the dynamic range to a non-zero value. Following normalization, in step 315 the digital representation of the structure 400 is collapsed parallel to extended run lines 405, or transformed along a first axis, to create a one-dimensional array of data representing all of the features of structure 400, as is seen in the array value representation 401 (array correspondence to features 405, and 410 shown by dotted lines connecting features in 400). This is done to enable identification, in step 320, of each extended run line 405, determine the spatial extent of each extended run line 405, and to discriminate out short run lines 410 and other features such as troughs 415 that are not extended run lines 405 and are therefore not a portion of the structure of interest for void detection. An embodiment of the present disclosure also provides for detection of short run lines 410 in much the same manner as for that of extended run lines 405. In the case of a sheet of film or a portion of a sheet of film being used as the resolution device, in place of extended run lines 405, the user could define "virutal" long run lines (not illustrated) to apply the techniques taught herein. These virutal long runs would be analogous to a contiguous series of extended run lines 405 and would possess dimensionality (a thickness), thus enabling application of the method as disclosed by the present invention.

Following identification of extended run lines 405 in step 320, in step 325, an additional transformation is accomplished by collapsing the information of each extended run line 405 orthogonal to extended run line 405 into a second one-dimensional array in order to locate the voids. This permits analysis of the cross sectional areas of extended run lines 405 in step 330. The analysis of step 330 consists of subtracting the dc and low frequency components (slowly varying background) by applying a smoothing technique, e.g., an n-point moving average from the line values in the second array, where n=a desired integer for the smoothing interval, i.e., 5, 10, 25, et cetera, then subtracting this smoothed version of the line from the original line data. The system then executes instructions to identify all points in the processed data that are below some threshold. The points below the threshold are voids. The cross sections through each void are then analyzed to determine if the void is a complete void or a partial void by setting a threshold value. If a point value is greater than the threshold value, this represents a partial void. Point values above the threshold are full voids.

After void detection and categorization in step 330, the voids are counted in step 335. In step 340, the void count output is displayed. The void count output can be displayed in various ways, for example, a presentation in tabular format in a spreadsheet, or a digital representation (modified photomicrograph) showing the void locations. Void data can be selectively filtered such that a display of output could include total number of voids, full voids only, partial voids only, full voids for a particular time split, or other such options. The void output display filtering capability of the present invention provides yield management engineers with additional flexibility for trend analysis of a

process.

The various functions and components in the present application may be implemented using an information-handling machine such as a data processor, or a plurality of processing devices. Such a data processor may be a microprocessor, microcontroller, microcomputer, digital signal processor, state machine, logic circuitry, and/or any device that manipulates digital information based on operational instruction, or in a predefined manner. Generally, the various functions, and systems represented by block diagrams are readily implemented by one of ordinary skill in the art using one or more of the implementation techniques listed herein.

When a data processor for issuing instructions is used, the instruction may be stored in memory. Such a memory may be a single memory device or a plurality of memory devices. Such a memory device may be a read-only memory device, random access memory device, magnetic tape memory, floppy disk memory, hard drive memory, external tape, and/or any device that stores digital information. Note that when the data processor implements one or more of its functions via a state machine or logic circuitry, the memory storing the corresponding instructions may be embedded within the circuitry that includes a state machine and/or logic circuitry, or it may be unnecessary because the function is performed using combinational logic.

The method and apparatus herein provides for a flexible implementation. Although the invention has been described using certain specific examples, it will be apparent to those skilled in the art that the invention is not limited to these few examples. For example, the disclosure is discussed herein primarily with regard to void detection in the SEM voltage contrast mode, however, the invention can be used in other modes or processes that use beams of energetic, charged particles, such as electron beam induced current isolation (EBIC) imaging systems. Additionally, various types of electron beam devices are currently available which could be suitable for use in employing the method as taught herein, e.g., HVSEM, TEM, STEM, and the like. Note also, that although an embodiment of the present invention has been shown and described in detail herein, along with certain variants thereof, many other varied embodiments that incorporate the teachings of the invention may be easily constructed by those skilled in the art. Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. Accordingly, the present invention is not intended to be limited to the specific form set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents, as can be reasonably included within the spirit and scope of the invention.

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